

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization  
International Bureau



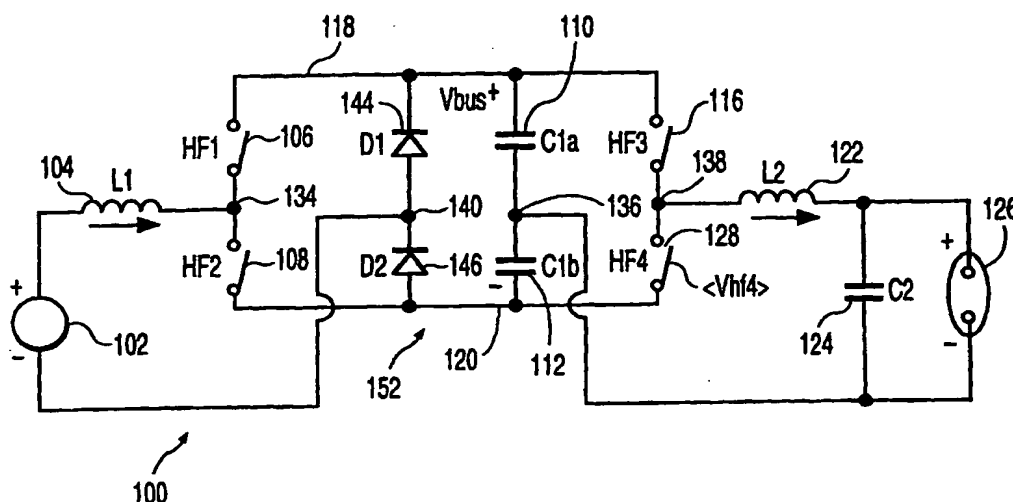
(43) International Publication Date  
10 May 2001 (10.05.2001)

PCT

(10) International Publication Number  
**WO 01/33915 A1**

- (51) International Patent Classification<sup>7</sup>: **H05B 41/00** (74) Agent: **DUSSELDORP, Jan, C.**; Internationaal Octrooibureau B.V., Prof Holstlaan 6, NL-5656 AA Eindhoven (NL).
- (21) International Application Number: **PCT/EP00/10002**
- (22) International Filing Date: **10 October 2000 (10.10.2000)** (81) Designated States (*national*): **CN, JP.**
- (25) Filing Language: **English** (84) Designated States (*regional*): **European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).**
- (26) Publication Language: **English**
- (30) Priority Data:  
**09/431,582 1 November 1999 (01.11.1999) US**
- (71) Applicant: **KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).**
- (72) Inventor: **SHEN, Eric; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).**
- Published:**  
— *With international search report.*  
— *Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.*
- For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: **A HIGH POWER FACTOR ELECTRONIC BALLAST WITH SIMPLIFIED CIRCUIT TOPOLOGY**



(57) Abstract: An electronic ballast circuit for driving a gas discharge lamp from a mains voltage signal supply includes a ballast bridge unit having upper and lower signal lines. A capacitive divider is disposed across the bridge. The capacitive divider comprises at least two capacitors coupled in series at a common reference voltage signal terminal. The bridge unit also includes two diodes coupled in series at a rectifier common terminal, wherein each of the diodes is respectively coupled to one of the signal lines of the bridge unit. The bridge unit further includes an input converter bridge and an output converter bridge each having at least two switches coupled in series at an input and output common terminals, respectively.

WO 01/33915 A1

## A high power factor electronic ballast with simplified circuit topology

This invention relates to an electronic ballast circuit and more specifically to a ballast arrangement employed for driving High Intensity Discharge (HID) lamps with a signal having a controllable frequency.

5

There is an ever increasing need for gas discharge lamps, such as fluorescent lamps for both commercial and consumer applications. Gas discharge lamps are usually driven by a mains voltage supply source provided by power utility companies. In order to drive a discharge lamp from the mains voltage supply line, a ballast is employed that functions as an interface between the lamp and the supply line.

One main function of a ballast is to drive the discharge lamp with a signal that has an appropriate voltage and current level. Another important function of a ballast is to perform, what is known as, power factor correction. The voltage and current level necessary to operate the discharge lamp is governed, among other things, by the characteristics of gas contained inside the lamp. Power factor correction is necessary to insure that the operation of the ballast does not contribute noise signals to the power supply line feeding the ballast. Typically, a power factor correction arrangement controls the supply current provided by the ballast such that it remains in phase with the voltage supply line waveform.

With the advent of HID lamps, the ballast's need to also ensure that the discharge lamp is driven by a low frequency current signal, in the range of 1kHz or less. Driving an HID lamp at high frequencies is usually difficult due to arc instabilities caused by acoustic resonance. This resonance can lead to lamp failure.

Fig. 1 illustrates a circuit diagram of a typical ballast 10 employed to drive an HID lamp. The operation of ballast 10 is very well understood and is not described in detail herein. The ballast circuit includes an upper signal line and a lower signal line each coupled to a respective terminal of mains power supply line. Ballast 10 comprises an EMI filter 36 followed by a full bridge diode rectifier 12 to rectify the ac voltage signal provided by the mains supply line. The rectified signal is then fed to a preconditioner stage, such as a boost converter 14, which operates to shape the ballast supply current, also referred to as mains

current, for power factor correction. The preconditioner is followed by an energy storage capacitor 26, which accumulates a dc bus voltage  $V_{bus}$ , which is typically larger than the peak voltage level provided by the mains power supply line. Boost converter 14 includes an inductor 20 having inductance  $I_L$ , along the upper signal line of ballast 10, coupled in series with a diode 24, which in turn is coupled to storage capacitor 26. A transistor switch 22 is coupled across inductor 20 and lower signal line of the ballast. The duty cycle of switch 22 can be controlled so as to operate the boost converter in different operation modes.

For example, boost converter 14 can operate under, what is known as, a continuous conduction mode operation (CCM). During this mode of operation, the average voltage across capacitor 26 is  $V_{26} = V_{in} / (1 - D(t))$  wherein  $V_{in}$  is the voltage signal fed to boost converter 14 and  $D(t)$  a variable duty cycle of switch 22. A controller (not shown) varies the duty cycle of switch 22 so that the current  $I_L$  has a sinusoidal shape that is in phase with the mains voltage supply waveform. Other control operation modes for boost converter 14 include discontinuous conduction mode operation (DCM) and critical discontinuous conduction mode operation (CDCM), which may be employed based on various design considerations. For a continuous conduction mode operation, the average voltage signal across inductor 20 is substantially zero.

Boost converter 14 is followed by a buck converter 16 that is fed by the dc bus voltage signal formed across capacitor 26. A transistor switch 28 couples capacitor 26 to an inductor 32, which in turn is coupled to a filter capacitor 34. A diode 30 is coupled across switch 28 and lower signal line of the ballast. The buck converter creates a dc current which drives the lamp through a commutator stage 18.

Commutator stage 18 includes four transistor switches, which interchangeably operate to switch the current signal provided to lamp 36. The commutator inverts the lamp polarity at a low frequency, typically in the 100Hz range.

One disadvantage with the ballast circuit described in Fig. 1 is that it suffers from a high component count and poor converter efficiency. There has been some effort to reduce the number of component parts of a ballast for driving HID lamps. One approach is to synchronize the lamp current to the power supply voltage frequency, as described in United States Patent No. 5,917,290, entitled Parallel-Storage Series-Drive Electronic Ballast. The disadvantage with such a ballast circuit is that when the frequency of the power voltage supply signal is low, for example 50Hz, there is the possibility of a visible light flicker from the lamp.

Thus, there is a need for an efficient and simple ballast circuit, having a low component count and a driving current signal that has a controllable frequency to avoid possible light flicker.

5

In accordance with one embodiment of the invention an electronic ballast circuit includes a ballast bridge unit configured to receive a ballast supply signal from a mains voltage supply line via an input inductor. The ballast bridge unit comprises an input converter bridge having at least two switches, preferably transistor switches coupled in series at a common terminal, wherein an upper transistor switch is coupled to the upper signal line of the ballast bridge unit and the lower transistor switch is coupled to the lower signal line of the ballast bridge unit. The transistor switches of the input converter bridge are operated such that the input converter current waveform follows the mains voltage supply signal waveform.

The ballast bridge unit includes a rectifier bridge comprising of two diodes coupled in series forming a diode bridge common terminal. The upper diode is coupled to the upper signal line of the bridge unit, while the lower diode is coupled to the lower signal line of the bridge unit.

The ballast bridge unit further comprises an output converter bridge having at least two switches, preferably two transistors switches coupled in series at an output common terminal, wherein an upper transistor switch is coupled to the upper signal line of the ballast bridge unit and the lower transistor switch is coupled to the lower signal line of the ballast bridge unit. The transistor switches of the output converter bridge are operated such that the average voltage signal level of their common output terminal shifts between two desired values, so as to form an ac current for driving a gas discharge lamp.

The ballast bridge unit also comprises a capacitor divider bridge having at least two storage capacitors coupled in series at a reference voltage common terminal, wherein an upper storage capacitor is coupled to the upper line of the ballast bridge unit and the lower storage capacitor is coupled to the lower signal line of the ballast bridge unit. The voltage across the two storage capacitors defines a bus voltage signal,  $V_{bus}$ , for the input and output converters of the ballast circuit. The average voltage signal level of the reference voltage terminal is set at half the bus voltage signal so as to form a differential voltage signal between the output common terminal and the common reference voltage terminal.

The output common terminal of the ballast bridge unit is coupled to a filter capacitor via an output inductor so as to provide a driving signal to a gas discharge lamp disposed across the filter capacitor.

5 During operation, the input converter bridge switches are controlled at a high frequency in a pulse width modulation arrangement to shape the input inductor current to be in phase with the mains voltage signal. The diodes in the rectifier bridge work together with input converter bridge switches to rectify the mains voltage signal.

The switches of the output converter bridge successively operate in an active arrangement for a desired period of time so as to provide an ac current signal to a gas  
10 discharge lamp that is driven by the electronic ballast circuit. Advantageously, the frequency within which the active operation of the switches successively changes defines the frequency of the current signal that drives the gas discharge lamp.

The arrangement of the ballast circuit in accordance with the principles of the present invention provides for a simple design with a low component part and high efficiency  
15 that generates a lamp driving current that has a desirable frequency above a range that causes visible light to flicker.

In accordance with another embodiment of the invention the ballast bridge unit also includes a low frequency voltage reference bridge having a reference voltage terminal that provides a shifting voltage differential between the output common terminal of output  
20 converter bridge and the reference voltage terminal.

Fig. 1 illustrates a circuit diagram of a prior art ballast circuit for driving a high intensity discharge lamp.

25 Fig. 2 illustrates a circuit diagram of a ballast circuit in accordance with one embodiment of the invention.

Fig. 3 illustrates a circuit diagram of a ballast circuit in accordance with another embodiment of the invention.

Figs. 4(a)-4(d) are plots of waveforms representing signals generated by the  
30 ballast circuit illustrated in Fig. 2 providing a 120Hz output frequency.

Figs. 5(a)-5(d) are plots of waveforms representing signals generated by the ballast circuit illustrated in Fig. 2 providing a 200 Hz output frequency.

Fig. 2 illustrates an electronic ballast circuit 100 in accordance with one embodiment of the present invention. Voltage supply source 102 represents the mains ac power supply voltage signal. Voltage supply source 102 is coupled to an input inductor 104 having an inductance  $L_1$ . Input inductor 104 is coupled to a ballast bridge unit 132.

5 Ballast bridge unit 132 includes an input converter bridge that contains two high frequency switches 106 and 108 coupled in series. The input common terminal 134 of the input converter bridge is coupled to inductor 104. Upper switch 106 is coupled to the upper signal line 118 of the ballast bridge unit, whereas the lower switch 108 is coupled to the lower signal line 120 of the ballast bridge unit.

10 Ballast bridge unit 132 also includes a capacitor bridge that comprises a capacitive divider made of two capacitors 110 and 112 coupled in series at a common reference voltage terminal 136. The other terminal of capacitor 110 is coupled to upper signal line 118 of ballast bridge unit 132. The other terminal of capacitor 112 is coupled to lower signal line 120 of the ballast bridge unit 132. The voltage across the two capacitors 110 and 112 defines a bus voltage,  $V_{bus}$ , employed by the input and output converters of ballast circuit 100 in accordance with one embodiment of the present invention.

Ballast bridge unit 132 further includes an output converter bridge that contains two high frequency switches 116 and 128 coupled in series. The output common terminal 138 of the output converter bridge is coupled to an output inductor 122. Upper switch 116 is coupled the upper signal line 118 of the ballast bridge unit, whereas the lower switch 128 is coupled to the lower signal line 120 of the ballast bridge unit.

25 Finally, ballast bridge unit 132 includes a rectifier bridge that contains two diodes 144 and 146 coupled in series. The bridge common terminal 140 is coupled to one terminal of mains voltage signal source 102. The cathode terminal of diode 144 is coupled to the upper signal line of ballast bridge unit 132, while the anode terminal of diode 146 is coupled to the lower signal line of the ballast bridge unit.

Ballast circuit 100 further includes a filter capacitor 124 and a lamp 126 coupled in parallel, configured to be driven by the current provided through output inductor 122, which has an inductance  $L_2$ . One terminal of lamp 126 is coupled to inductor 122, while 30 its other terminal is coupled to common reference voltage terminal 136.

It is noted that the input stage of ballast circuit 100 includes the two switches 106 and 108 and inductor 104, which together form an input converter for regulating the input supply current. The input convert functions similarly to a boost converter. Diodes 144

and 146 are typically low frequency diodes which work together with switches 106 and 108 to rectify the voltage signal provided by mains voltage signal source 102. The output stage of ballast circuit 100 includes the two high frequency switches 116 and 128 and inductor 122 which form an output converter employed to regulate the output current that drives gas discharge lamp 126. The output converter functions similarly to a buck converter. As explained above, capacitors 110 and 112 together form a voltage storage capacitor, for storing voltage signal  $V_{bus}$  as employed by the input converter input stage and the output converter output stage.

During operation, high frequency switches 106 and 108 are operated at a high frequency, for example 100kHz, with inductor 104 to regulate the current signal flowing through input inductor 104. When the mains voltage signal generated by voltage signal source 102 has a positive level, and current signal  $I_{L1}$  flowing through inductor 104 is also positive, diode 146 is forward biased. In this case, switch 108 which is activated, performs the function of the input converter transistor and switch 106, which is deactivated, performs the function of the input converter diode. Alternatively, when the mains voltage signal generated by voltage signal source 102 has a negative level, the current signal  $I_{L1}$  flowing through inductor 104 is negative and diode 144 is forward biased. In this case switch 106, which is activated, performs the function of the input converter transistor and switch 108, which is deactivated, performs the function of the input converter diode.

In accordance with one embodiment of the invention, the input converter is operated under continuous conduction mode (CCM) described above. For this operation, diodes 144 and 146 may be low frequency diodes. This follows, because the diodes are alternatively forward biased at a frequency substantially equal to the frequency of the mains voltage signal.

On the load side of ballast circuit 100, switches 116 and 128 are operated at a high frequency pulse width modulated arrangement to shape the current signal flowing through inductor 122 as a low frequency square wave. It is noted that the frequency of the driving current signal may be a specifiable frequency depending on the operation of switches 116 and 128 as described hereinafter.

In accordance with one embodiment of the present invention, both the input converter and the output converter of ballast circuit 100 operate under continuous conduction mode (CCM) operation. Thus, if the duty cycle of switch 116 is  $D1$  then the average voltage signal at common output terminal 138 labeled <vhf4> is  $D1 \times V_{bus}$ .

For example, if the voltage signal,  $V_{bus}$ , across capacitors 110 and 112 is 300 Volts and the voltage signal at the reference voltage terminal 136 is 150 Volts, to generate a lamp voltage of 100Volts, the duty cycle of switch 116 is chosen so that the average voltage across switch 128 is 250 Volts. This follows, because the difference between the average  
5 voltage signal across switch 128 and the reference voltage terminal of capacitive bridge is substantially equal to the lamp voltage. The average voltage potential across inductor 122 is substantially zero for continuous conduction mode (CCM) operation. Similarly, in order to generate a lamp voltage of -100 Volts, the duty cycle of switch 116 is chosen such that the average voltage across switch 128 is 50 Volts. While continuous conduction mode (CCM)  
10 operation has been described for purposes of illustration, the invention embodied in ballast circuit 100 is not limited in scope in that respect. For example, the ballast circuit may be operated in discontinuous conduction mode or critical discontinuous conduction mode.

The lamp polarity may be shifted, or inverted, at any frequency, independent of the frequency of the mains voltage supply signal. All that is necessary is to activate switch  
15 116 for a specifiable period of time, while switch 128 is deactivated, and conversely, activate switch 128 for a specifiable period of time, while switch 116 is deactivated.

It is noted that in order for the ballast circuit arrangement of Fig. 2 to operate properly so as to generate the required voltage signals, bus voltage signal,  $V_{bus}$ , must be greater than either the peak level of the mains voltage signal or twice the lamp voltage signal,  
20 whichever is greater.

Thus in accordance with the principles of the present invention, ballast circuit 100 achieves desired driving voltage and current signals with specifiable frequency with substantially lower component count than the prior art ballast circuit illustrated in Fig. 1. Furthermore, the combined voltage rating for the storage capacitors 110 and 112 is on the  
25 order of either the peak level of the mains voltage or about twice the lamp voltage.

With the capacitive divider bridge illustrated in Fig. 2, the available voltage signal to lamp 126 is half of bus voltage signal,  $V_{bus}$ . However, there may be applications that the required voltage signal for lamp 126 is substantially high. In that event, the voltage rating of capacitors 110 and 112 will be correspondingly higher.

30 Fig. 3 illustrates a ballast circuit 200 in accordance with another embodiment of the invention, which increases the available voltage to lamp 126 as compared to ballast circuit 100 (Fig. 2). Specifically, in ballast circuit 200 capacitive divider of ballast bridge unit is replaced by a low frequency reference voltage bridge that contains two low frequency



switches 222 and 224 coupled in series having a reference common terminal 236. Upper switch 222 is coupled to upper signal line 118 of bridge unit 232, while the lower switch 224 is coupled to the lower signal line 120 of bridge unit 232. Furthermore, a storage capacitor 220 is coupled across bridge unit 232, having one terminal coupled to the upper signal line of the bridge unit and the other terminal coupled to the lower signal line of the bridge unit, so as to accumulate a bus voltage signal,  $V_{bus}$ .

During operation, when switch 224 is activated, switch 116 is activated to perform the function of an output transistor switch, while switch 128 is deactivated to perform the function of an output converter diode. As a result, positive current and voltage signals are delivered to lamp 126. Similarly, when switch 222 is activated, switch 128 is activated to perform the function of an output transistor switch, while switch 116 is deactivated to perform the function of an output converter diode. As a result, negative current and voltage signal are delivered to lamp 126. Therefore, the available voltage to be delivered to the lamp 126 is on the order of the bus voltage  $V_{bus}$  in both positive and negative polarities. The rate with which transistor switches 222 and 224 are alternatively activated and deactivated defines the frequency of voltage and current signals that drive lamp 126.

Figs. 4a - 4d illustrate the waveforms generated in connection with the operation of an electronic ballast circuit, such as the one illustrated in Fig. 2. Specifically, Fig. 4a illustrates voltage signal  $V_{bus}$  which is set to about 400 Volts, and the voltage signal provided by mains power supply line. As illustrated, the mains voltage signal swings between positive and negative 170 Volts. The output frequency of the signal driving lamp 126 is configured to be 120Hz.

Fig. 4(b) illustrates the current signal 302 flowing through input inductor 104, which is in phase with the mains voltage signal (Fig.4a).

Fig.4 ( c ) illustrates the lamp current signal flowing through inductor 122, while Fig. 4(d) illustrates the lamp voltage signal across capacitor 124.

Figs. 5(a)- 5(d) illustrate the waveforms generated in connection with the operation of the electronic ballast circuit, such as the one illustrated in Fig. 2, wherein the frequency of the driving signal is configured to be 200 Hz.

While only certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes or equivalents will now occur to those skilled in the art. It is therefore to be understood that the appended claims are intended to cover all such modifications and changes that fall within the true spirit of the invention.

## CLAIMS:

1. In an electronic ballast circuit (100) for driving a gas discharge lamp (126) from a mains voltage signal supply (102), a ballast bridge unit (152) having an upper and lower signal line (118), (120) comprises:
- a capacitive bridge having at least two capacitors coupled in series at a common reference voltage signal terminal (136), wherein one of said capacitors (110) is coupled to the upper signal line (118) of the bridge unit and another one of said capacitors (112) is coupled to the lower signal line of said bridge unit (120);
- a bridge having at least two diodes coupled in series at a rectifier bridge common terminal (140), wherein one of said diodes (144) is coupled to the upper signal line (118) of the bridge unit and another one of said diodes (146) is coupled to the lower signal line (120) of said bridge unit;
- an input converter bridge having at least two switches coupled in series at an input common terminal (134), wherein an upper switch (106) of said input converter bridge is coupled to the upper signal line (118) of the ballast bridge unit and the lower switch (108) of said input converter bridge is coupled to the lower signal line (120) of the ballast bridge unit; and
- an output converter bridge having at least two switches coupled in series at an output common terminal (138), wherein an upper switch (116) of said output converter bridge is coupled to the upper signal line (118) of the ballast bridge unit and the lower switch (128) is coupled to the lower signal line (120) of the ballast bridge unit.
2. The invention in accordance with claim 1, wherein said common terminal (134) of said input converter bridge is coupled to an input inductor (104), and said common terminal (138) of said output converter bridge is coupled to an output inductor (122) and said common terminal of said rectifier bridge common terminal (140) is coupled to one terminal of a mains voltage signal supply line, and said common reference voltage signal terminal (136) is coupled to one terminal of said gas discharge lamp (126).

3. The invention in accordance with claim 1, wherein said switch (116) of said output converter bridge coupled to the upper signal line (118) of said bridge unit is activated and deactivated at a frequency defining the frequency of current signal driving the gas discharge lamp (126).

5

4. The invention in accordance with claim 3, wherein said switch (128) of said output converter bridge coupled to the lower signal line (120) of said bridge unit is deactivated while the corresponding switch unit (116) coupled to the upper signal line (118) of said bridge unit is activated and vice versa.

10

5. The invention in accordance with claim 1 wherein the voltage signal level across said capacitive bridge capacitors is substantially equal to a greater of peak mains voltage supply and peak to peak lamp voltage swing.

15

6. In an electronic ballast circuit (200) for driving a gas discharge lamp (126) from a mains voltage signal supply (102), a ballast bridge unit (232) having an upper and lower signal line (118), (120) comprises:

a storage capacitor (220) coupled across said upper and lower bridge unit signal lines;

20

an input converter bridge having at least two switches coupled in series at an input common terminal (134), wherein an upper switch (106) of said input converter bridge is coupled to the upper signal line (118) of the ballast bridge unit and the lower switch (108) of said input converter bridge is coupled to the lower signal line (120) of the ballast bridge unit; and

25

an output converter bridge having at least two switches coupled in series at an output common terminal (138), wherein an upper switch of said output converter bridge is coupled to the upper signal line (118) of the ballast bridge unit and the lower switch is coupled to the lower signal line (120) of the ballast bridge unit;

30

a low frequency reference voltage bridge having at least two switches coupled in series at common reference voltage terminal (236), wherein an upper switch (222) of said reference voltage bridge is coupled to the upper signal line (118) of the ballast bridge unit and the lower switch (224) of said reference voltage bridge is coupled to the lower signal line (120) of the ballast bridge unit; and

a rectifier bridge having at least two diodes coupled at a common rectifier bridge terminal (140), wherein an upper diode (144) of said rectifier bridge is coupled to the upper signal line (118) of the ballast bridge unit and the lower diode (146) of said rectifier bridge is coupled to the lower signal line (120) of the ballast bridge unit.

5

7. The invention in accordance with claim 1 or 6 wherein said switches of said input and output converter bridges are high frequency switching transistors.

8. The invention in accordance with claim 6 or 7, wherein said common terminal (134) of said input converter bridge is coupled to an input inductor (104), and said common terminal (138) of said output converter bridge is coupled to an output inductor (122) and said common terminal (236) of said reference voltage signal bridge is coupled to one terminal of said gas discharge lamp and said common terminal (140) of rectifier bridge is coupled to one terminal of a mains power supply line.

15

9. The invention in accordance with claim 6 or 7, wherein said switch (116) of said output converter bridge coupled to the upper signal line (118) of said bridge unit and said switch (224) of said low frequency reference voltage bridge coupled the lower signal line (120) of said bridge unit are activated and deactivated at a frequency defining the frequency of current signal driving the gas discharge lamp (126).

20

10. The invention in accordance with claim 9, wherein each of said switch (128) of said output converter bridge coupled to the lower signal line (120) of said bridge unit and said switch (222) of said low frequency reference voltage bridge coupled to the upper signal line (118) of said bridge unit is deactivated while the corresponding switch unit of each of said bridges is activated and vice versa.

25

11. The invention in accordance with claim 6 or 7 wherein the voltage signal level across said bridge capacitor (220) is substantially equal to a greater of peak mains voltage supply swing and peak to peak lamp voltage swing.

30

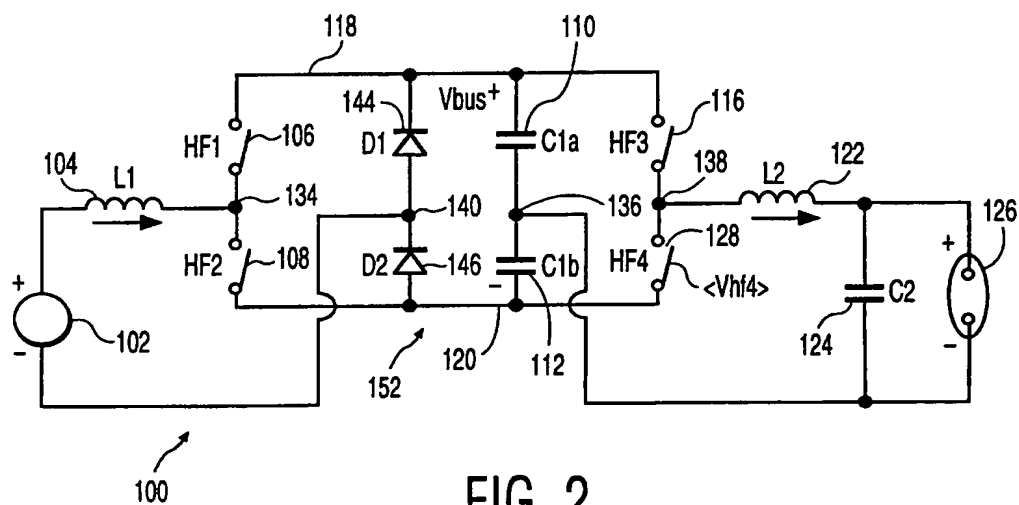
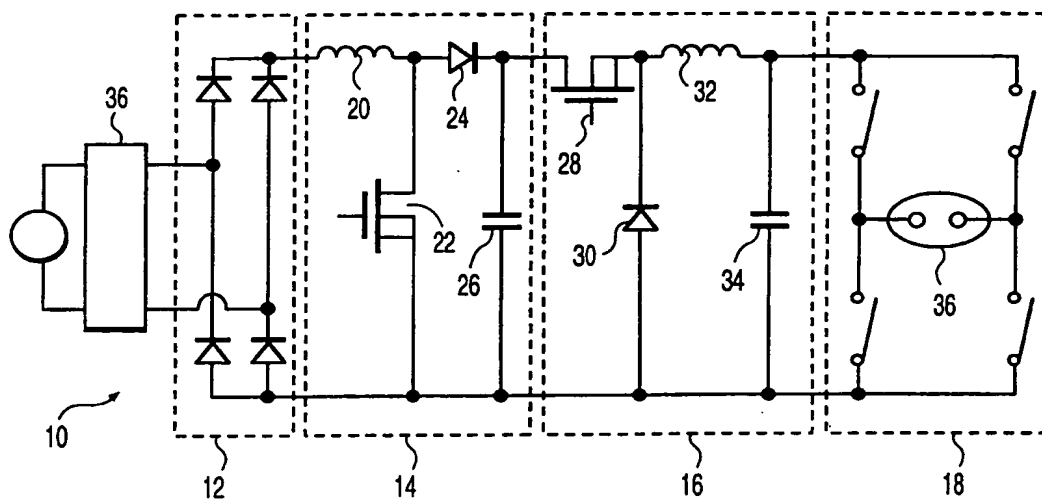
12. In a ballast circuit (100) for driving a gas discharge lamp (126) from a mains voltage supply line (102), said ballast circuit having a ballast bridge unit (152) having an input converter bridge (106), (108) coupled in parallel with an output converter bridge (116),

(128), a reference voltage signal bridge (110), (112), and a rectifier bridge (144), (146), a method for operating said ballast circuit comprising the steps of:

forming a voltage bus signal  $V_{bus}$  across a capacitive divider (110), (112) of said reference voltage signal bridge; and

- 5                   shifting an average voltage signal at a common output terminal (138) between two desired levels so as to form an ac current for driving the gas discharge lamp (126).

1/4



2/4

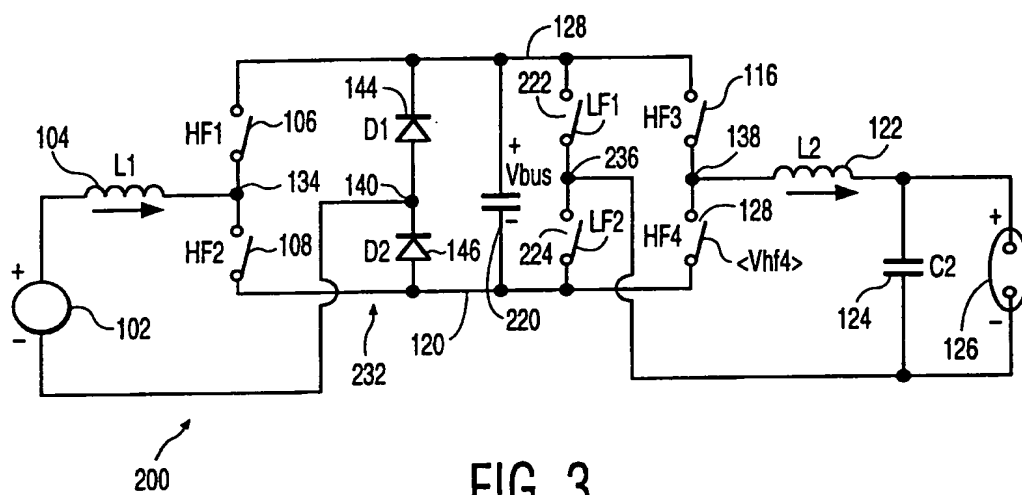


FIG. 3

3/4

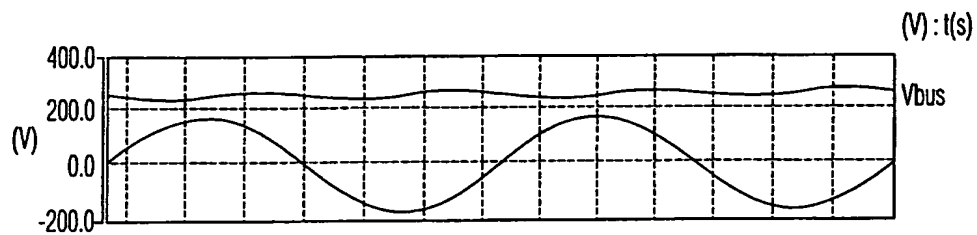


FIG. 4a

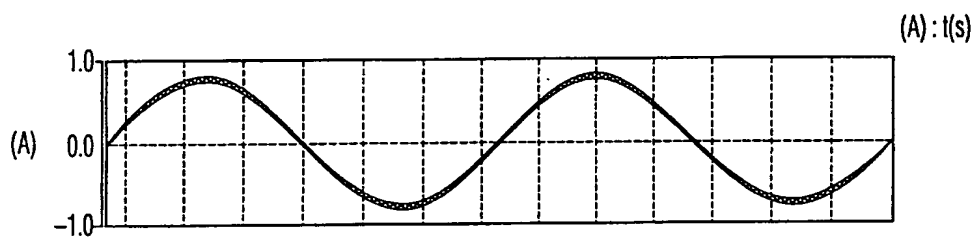


FIG. 4b

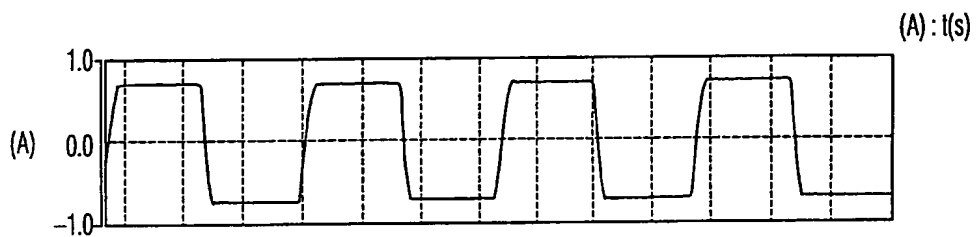


FIG. 4c

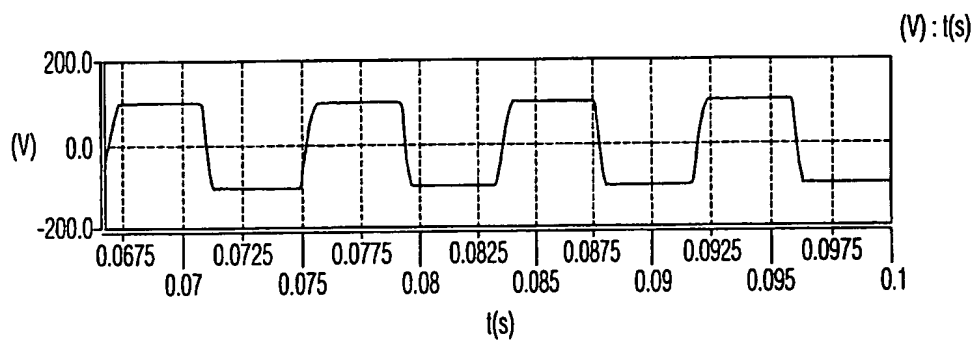


FIG. 4d



4/4

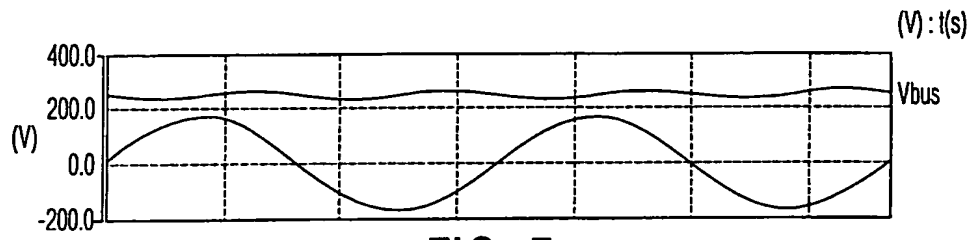


FIG. 5a

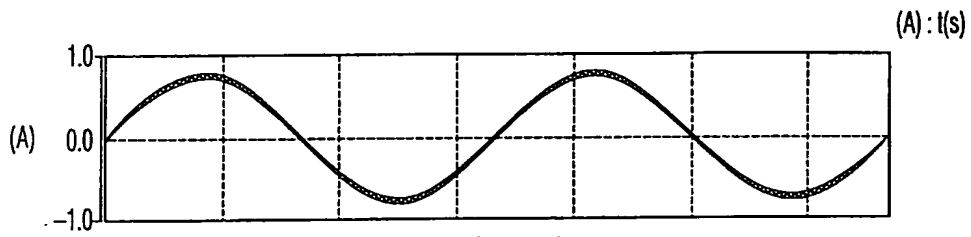


FIG. 5b

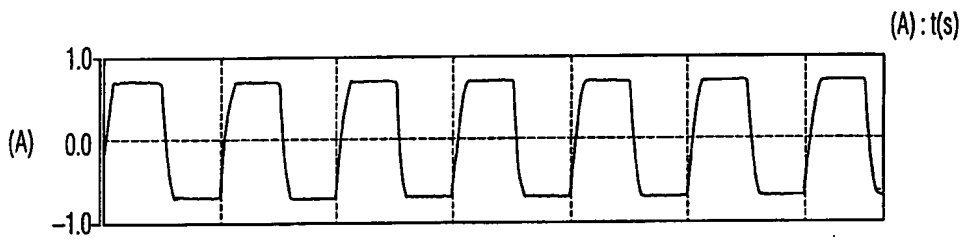


FIG. 5c

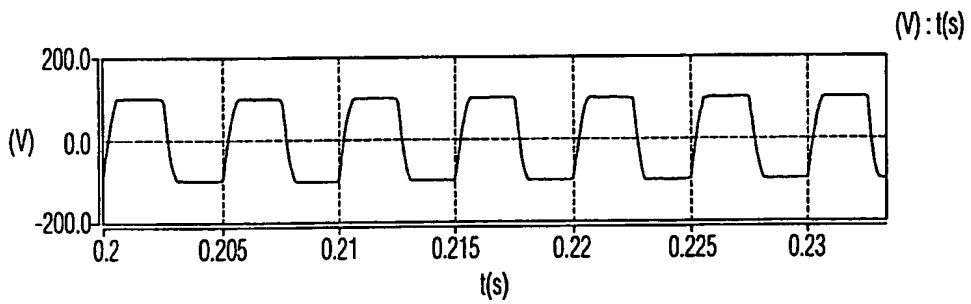


FIG. 5d

# INTERNATIONAL SEARCH REPORT

International Application No  
PCT/EP 00/10002

<b>A. CLASSIFICATION OF SUBJECT MATTER</b> IPC 7 H05B41/00		
According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b> Minimum documentation searched (classification system followed by classification symbols) IPC 7 H05B		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practical, search terms used)		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 459 651 A (MAEHARA MINORU) 17 October 1995 (1995-10-17) column 9, line 57 -column 10, line 13; figure 11	1-5,12
Y	--- US 5 917 290 A (SCHLECHT MARTIN FREDERICK ET AL) 29 June 1999 (1999-06-29) cited in the application column 9, line 47 -column 9, line 65; figure 13	1-5,12
A	--- PATENT ABSTRACTS OF JAPAN vol. 1999, no. 13, 30 November 1999 (1999-11-30) & JP 11 235054 A (MATSUSHITA ELECTRIC WORKS LTD), 27 August 1999 (1999-08-27) abstract --- -/--	1-5,12
<input checked="" type="checkbox"/> Further documents are listed in the continuation of box C. <input checked="" type="checkbox"/> Patent family members are listed in annex.		
* Special categories of cited documents :		
"A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search  17 January 2001		Date of mailing of the international search report  15.03.01
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016		Authorized officer  VILLAFUERTE ABR., L

# INTERNATIONAL SEARCH REPORT

International Application No  
PCT/EP 00/10002

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,P	US 6 034 489 A (WENG DA FENG) 7 March 2000 (2000-03-07) the whole document	1-5,12
A	DE 33 34 829 A (ERZMONEIT HORST;WOLF KARL) 11 April 1985 (1985-04-11) the whole document	1-5,12
A	EP 0 667 734 A (MAGNETEK SPA) 16 August 1995 (1995-08-16) the whole document	1-5,12
A	WO 99 25158 A (KONINKL PHILIPS ELECTRONICS NV ;PHILIPS SVENSKA AB (SE)) 20 May 1999 (1999-05-20) the whole document	1-5,12

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/EP 00/10002

### Box I Observations where certain claims were found unsearchable (Continuation of Item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:  
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:  
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
3. ☐ Claims Nos.:  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

### Box II Observations where unity of invention is lacking (Continuation of Item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-5, 12

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
- ☐ No protest accompanied the payment of additional search fees.

# INTERNATIONAL SEARCH REPORT

International Application No. PCT/EP 00/10002

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

1. Claims: 1-5, 12

Ballast with capacitive bridge.

2. Claims: 6-11

Ballast with storage capacitor and a low frequency reference voltage bridge.

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/EP 00/10002

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5459651 A	17-10-1995	JP 3085703 B	11-09-2000
		JP 4193067 A	13-07-1992
		JP 5056660 A	05-03-1993
		JP 5056647 A	05-03-1993
		CA 2056010 A,C	23-05-1993
		DE 69117008 D	21-03-1996
		DE 69117008 T	01-08-1996
		EP 0488478 A	03-06-1992
		KR 9605690 B	30-04-1996
		US 5274540 A	28-12-1993
		CA 2058207 A,C	26-06-1992
		DE 69118501 D	09-05-1996
		DE 69118501 T	26-09-1996
		EP 0492715 A	01-07-1992
		KR 145690 B	01-10-1998
		US 5251119 A	05-10-1993
US 5917290 A	29-06-1999	CN 1249896 T	05-04-2000
		EP 0948878 A	13-10-1999
		WO 9925159 A	20-05-1999
JP 11235054 A	27-08-1999	US 6034489 A	07-03-2000
US 6034489 A	07-03-2000	JP 11235054 A	27-08-1999
DE 3334829 A	11-04-1985	NONE	
EP 0667734 A	16-08-1995	AT 167019 T	15-06-1998
		CA 2142250 A	12-08-1995
		DE 69410775 D	09-07-1998
		DE 69410775 T	03-12-1998
		ES 2118355 T	16-09-1998
		US 5485060 A	16-01-1996
WO 9925158 A	20-05-1999	CN 1249895 T	05-04-2000
		EP 0951806 A	27-10-1999